

REMARKS

The present communication is responsive to the Official Action mailed May 16, 2005. A petition for a three-month extension of the term for response to the Official Action, to and including November 16, 2005, is transmitted herewith.

Claims 9-13, 17-21, 24-32 and 35-45 were rejected under 35 U.S.C. § 102(e) as assertedly anticipated by *Degani et al.*, U.S. Patent 6,734,539 B2 ("*Degani '539*"). Reconsideration is respectfully requested. The Examiner's detailed explanation as to how the teachings of *Degani '539* are applied in the rejection is appreciated.

As to independent claim 9, the Official Action (p. 3) asserts that *Degani '539* teaches an assembly with "at least some of said top connections being unoccupied and available to receive one or more additional microelectronic elements 75, 74." This statement is respectfully submitted to be erroneous. Elements 74 and 75 on top of substrate 76 are already mounted on the alleged bottom unit, i.e., the "interconnection substrate 76," and alleged bottom unit chip 74 below substrate 76. In the condition illustrated in FIG. 5 of the reference, chips 74 and 75 already occupy the supposed "top connections." By contrast, the plain language of claim 9 requires an assembly which includes both the circuit board and the bottom unit already assembled to the circuit board (note the language "at least some of said mounting connections being aligned with at least some of said contact pads"), and also requires that at least some of the top connections in this assembly be "unoccupied and available to receive one or more additional microelectronic elements." One example of such an assembly is shown in FIG. 3 of the present drawings. The bottom unit, including chip 54 (not numbered in FIG. 3; see FIG. 1) is already mounted on circuit board 70, and yet top connections 38, 36 remain unoccupied and available to

receive additional microelectronic elements. Nothing in the reference suggests that a subassembly including a chip 74 on the bottom of substrate 76 in *Degani* '539 FIG. 5 is mounted to the circuit board 73 before the chips 74 and 75 on the top surface are applied to substrate 76. The reference, accordingly, does not anticipate claim 9 or claims 10-13, dependent thereon.

As to independent claim 17, the Official Action asserts (p. 4) that elements 74 and 75 constitute "a first packaged semiconductor chip." It is respectfully submitted that this statement is contrary to the teachings of the reference. Elements 74 and 75 are "ICs, indicated at 74, and two more passive devices indicated at 75." (Col. 5, ll. 20-21.) Insofar as the reference discloses, these are bare, unpackaged devices. The entirety of the reference (e.g., col. 2, ll. 32-52; col. 4, l. 56 to col. 5, l. 5) refers to mounting and connection of "IC chips," i.e., bare unpackaged elements. FIG. 5 thus shows nothing more than mounting of bare unpackaged microelectronic elements on the top surface of substrate 76. By contrast, claim 17, paragraph (c), requires that the element having terminals overlying the top connection pads be "a first packaged semiconductor chip." As explicitly defined in the present specification (p. 17, ¶ 0038), "the term 'packaged semiconductor chip' refers to a unit including both the actual semiconductor element or 'bare die' itself and one or more components or layers which cover at least one surface or edge of the bare die." This is consistent with the common usage of the art, which draws a clear distinction between a bare die and a packaged chip. Thus, the asserted teachings in the reference do not meet paragraph (c) of the claim, and the anticipation rejection must be withdrawn. The same reasons apply with respect to claims 18-20 and 24-27, dependent on claim 17.

Independent claim 28 requires that the "bottom unit semiconductor chip" (paragraph (a)) be "permanently connected to

said substrate," whereas the "top microelectronic element" be "removably mounted to said substrate . . ." (paragraph (b)). Under any reasonable definitions of the terms "permanently" and "removably," this requires that the attachment between the top microelectronic element and the substrate be more readily detachable than the attachment between the bottom unit semiconductor chip and the substrate. Additionally, the specification (§ 0033) describes a permanent connection as one which "cannot be removed from the substrate simply by melting or breaking bonding material 64," and explicitly defines a "removable" connection as a connection "which can be removed without destroying the substrate" and hence one which is "thus more readily detachable than" the permanent attachment between the bottom unit chip and the substrate (§ 0043). Nothing of this sort has been pointed out in the teachings relied upon for rejection. Insofar as one can tell from the reference, chip 74 on the bottom of the substrate 76 (the asserted bottom unit semiconductor chip) is attached to the substrate in exactly the same way as elements 74 and 75 on the top surface of the substrates (the asserted top microelectronic elements). The structure, therefore, does not meet the "permanently connected" recitation of claim 28, paragraph (a), and the "removably mounted" recitation of claim 28, paragraph (b).

The same reasons apply with respect to claims 29-32 and 35-36, dependent from claim 28. Additionally, claim 29 specifically recites that the "first top microelectronic element" is a "packaged semiconductor chip." This claim thus further distinguishes over *Degani* '539 for the reasons pointed out above with respect to claim 17.

By the present amendment, claim 29 has been amended to correct a typographical error.

By the present amendment, claim 37 has been amended to incorporate the recitations of dependent claim 38, and

accordingly, dependent claim 38 has been canceled. Nothing in *Degani* '539 has been pointed out as properly teaching the surface areas of the bottom unit semiconductor chip or the first and second microelectronic elements. The drawings of *Degani* '539 are not drawn to scale, but instead are "schematic representation[s]." (See col. 1, l. 65 to col. 2, l. 9.) It is, accordingly, improper to measure or scale the drawings. Further, even if one could measure or scale the drawings of the reference, the relevant drawings are sectional views showing only the edges of elements 74 and 75, and not their front or rear surfaces. It is accordingly impossible to deduce the surface areas of these elements (the areas of their front or rear surfaces) from the drawings, even if one could scale them. For all of these reasons, the anticipation rejection should be withdrawn as to claim 37 and as to claims 39-45, dependent thereon.

Applicants submit herewith an Information Disclosure Statement.

As it is believed that all of the rejections set forth in the Official Action have been fully met by the foregoing amendments and remarks, favorable reconsideration and allowance of all pending claims are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

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Docket No.: TESSERA 3.0-328

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By 

Marcus J. Millet

Registration No.: 28,241

LERNER, DAVID, LITTENBERG,

KRUMHOLZ & MENTLIK, LLP

600 South Avenue West

Westfield, New Jersey 07090

(908) 654-5000

Attorney for Applicant

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